IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

DESIGN OF A HIGH-SPEED WALLACE TREE MULTIPLIER

Khushboo Bais*, Zoonubiya Ali
* Department of Electronics & Telecommunication Engineering, DIMAT, Raipur (C.G.), India

DOI: 10.5281/zenodo.55546

ABSTRACT

Multiplication is one of the most common arithmetic operations employed in digital systems, but multipliers are the most time, area, and power consuming circuits. Improvement in any of these parameters can be advantageous for improving the efficiency of the circuit. The ever increasing need for development of efficient and high speed multipliers has motivated several researchers to go a step ahead and present some novel approach. This paper presents an approach towards the reduction of delay in the Wallace tree multipliers by using 4:2 compressors along with full-adders and half-adders, in the partial product reduction stage; and employing Kogge-Stone adder for the final addition. The proposed multiplier has been designed using Xilinx ISE Design Suite 14.7 and implemented for Spartan 3 FPGA.

KEYWORDS: Wallace Tree Multiplier, 4:2 Compressor, Kogge-Stone Adder, Xilinx ISE, Spartan 3.

INTRODUCTION

Multipliers are an inevitable part of systems like ALUs, DSPs and other processors. They are often the slowest component of the circuit which limits the overall performance of the system. Hence, reduction of processing delay has been a major concern in research. Wallace tree multipliers are quite fast among the available multipliers [1], as they use the carry save addition algorithm [2], but with the ever-increasing demand for faster operations, attempts are being made to make it even faster.

The basic process of multiplication involves three essential steps: generation of partial products, reduction of the partial products, and summation of the reduced partial products in order to produce the final product [1], [3]. The overall delay of the multiplication process may be reduced by applying delay-reduction techniques in any or all of the three stages.

PROPOSED WALLACE TREE MULTIPLIER

The proposed scheme for delay reduction in multipliers focuses on minimising the delays occurring in the partial product reduction and final addition step of the multiplication process. The partial products for N-bit by N-bit multiplication have been generated by performing bit-by-bit AND operation of the two operands using N^2 AND gates [1], the partial product reduction phase utilises the combination of 4:2 compressors, full-adders and half-adders, and the final addition of the last two rows, to obtain the product, is achieved using a high speed Kogge-Stone adder. Figure 1 shows the multiplication of two 8-bit numbers. The multiplication has been extended for 16-bit and 32-bits operands using the decomposition algorithm presented in [4],[5], where four units of 8-bit by 8-bit multiplier have been combined to produce a 16-bit by 16-bit multiplier, and four units of the resulting 16-bit by 16-bit multiplier have been combined to give 32-bit by 32-bit multiplication result.

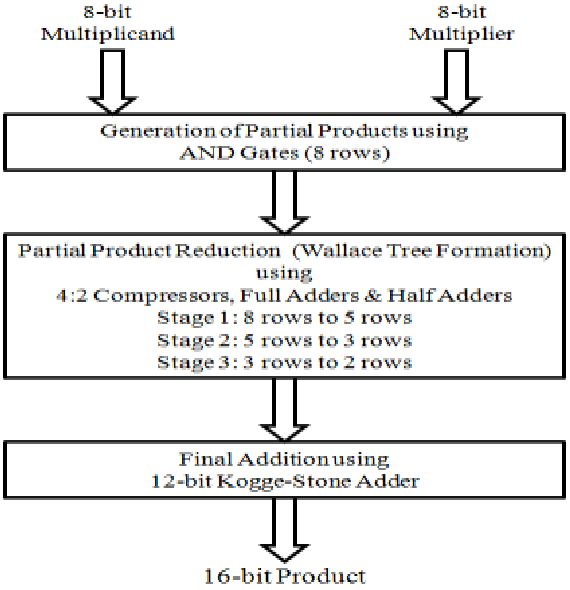
8-bit Multiplicand
8-bit Multiplier
Generation of Partial Products using AND Gates (8 rows)
Partial Product Reduction (Wallace Tree Formation) using 4:2 Compressors, Full Adders & Half Adders
Stage 1: 8 rows to 5 rows
Stage 2: 5 rows to 3 rows
Stage 3: 3 rows to 2 rows
Final Addition using 12-bit Kogge-Stone Adder
16-bit Product

Figure 1: Process Flow of 8-bit by 8-bit Multiplication

Compressor

The 4:2 compressor in [6] accepts four inputs- IN_1, IN_2, IN_3, IN_4, and a carry-in bit, C_{IN} and produces two outputs- SUM and CARRY, and a carry-out bit, C_{OUT}. Here, the circuit of compressor has been used as a column adder which adds five bits at a time giving three outputs- a sum (LSB) and two carry outputs (MSBs) of equal weight. Figure 2 [6] shows the 4:2 compressor, also called as 5:3counters in [7].

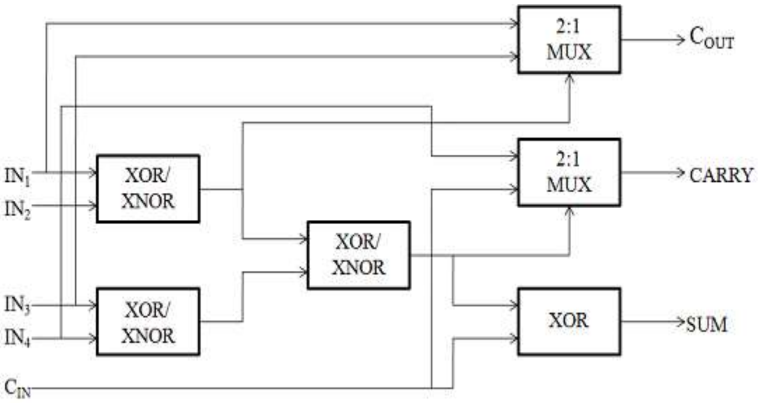

Figure 2: Architecture of 4:2 Compressor

The equations of output signals in [6], [8] are given as follows:

$$SUM = IN_1 \oplus IN_2 \oplus IN_3 \oplus IN_4 \oplus C_{IN} \quad (1)$$

$$CARRY = (IN_1 \oplus IN_2 \oplus IN_3 \oplus IN_4){\bullet}C_{IN} + \overline{(IN_1 \oplus IN_2 \oplus IN_3 \oplus IN_4)}{\bullet}IN_4 \quad (2)$$

$$C_{OUT} = (IN_1 \oplus IN_2){\bullet}IN_3 + \overline{(IN_1 \oplus IN_2)}{\bullet}IN_1 \quad (3)$$

The use of compressors in the partial product reduction stage has aided in minimising the number of stages needed to reduce the partial products to two, as compared with the conventional Wallace tree multiplier design described in [1]. For 8-bit multiplication, the conventional Wallace multiplication approach needs 4 stages for reduction of partial products as described in [1], [9], whereas the proposed approach achieves the target in 3 stages only.

Kogge-Stone Adder

The Kogge-Stone adder is a parallel prefix adder, known for its efficient and performance-oriented design. The diagram of the prefix stage of a 12-bit Kogge-Stone adder has been shown in figure 3 [10]. This adder generates all the carry signals in parallel using the generate signal G_i, and propagate signal, P_i, calculated using the i^{th} bit of input operands; thus reducing the computation delay. From the carry tree or prefix stage of the KSA we can calculate the carry signals using the relation in [10],

$$C_i = G_{i:0} \tag{4}$$

and the sum output will follow the relation in [10],

$$S_i = P_i \oplus G_{i-1:0} \tag{5}$$

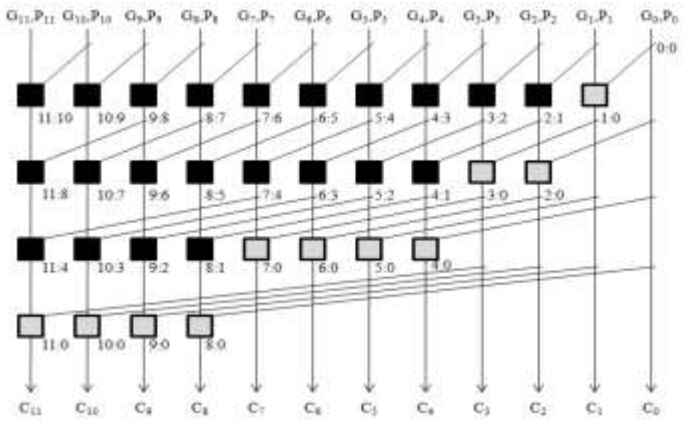

Figure 3: Generation of Carry Signals in 12-bit Kogge-Stone Adder

RESULT

The design entry of the proposed multiplier has been done in VHDL, using Xilinx ISE Design Suite 14.7; synthesis reports have been generated using XST for XC3S1500FG676-4 FPGA, and simulation results have been obtained by ISim simulator.

The delay analysis, and device utilization summary (after implementation) of 8-bit by 8-bit, 16-bit by 16-bit, and 32-bit by 32-bit multipliers have been described in Table 1 and Table 2, respectively.

Table 1: Delay Analysis of Multipliers

Delay (in ns)	**8-bit by 8-bit Multiplier**	**16-bit by 16-bit Multiplier**	**32-bit by 32-bit Multiplier**
Maximum Combinational Path Delay	28.601	51.090	88.114
Logic Delay	13.797	21.511	34.375
Route Delay	14.804	29.579	53.739

Table 2: Device Utilization Summary of Multipliers

Logic Utilization	**8-bit by 8-bit Multiplier**	**16-bit by 16-bit Multiplier**	**32-bit by 32-bit Multiplier**
No. of 4-input LUTs	181	819	3765
No. of Occupied Slices	97	444	2021
No. of Bonded IOBs	32	64	128
Average Fanout of Non-Clock Nets	3.45	3.44	3.53

The simulation results of the 8-bit by 8-bit, 16-bit by 16-bit, and 32-bit by 32-bit multipliers have been shown in figure 4, 5, and 6, respectively.

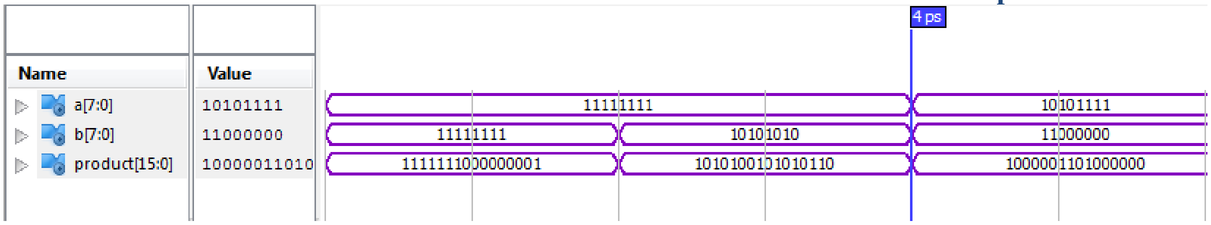

Figure 4: Waveform for 8-bit by 8-bit Multiplier

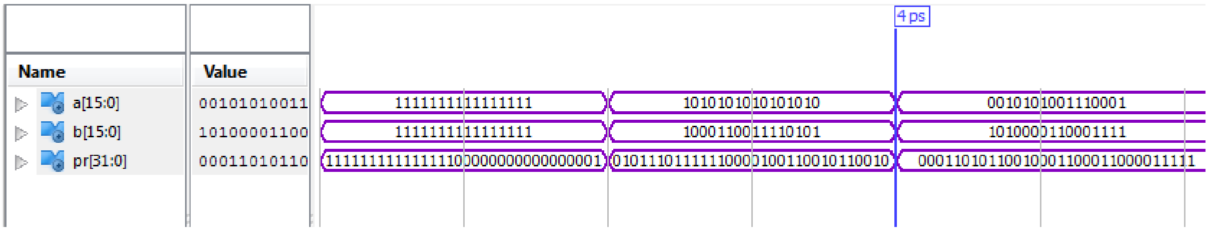

Figure 5: Waveform for 16-bit by 16-bit Multiplier

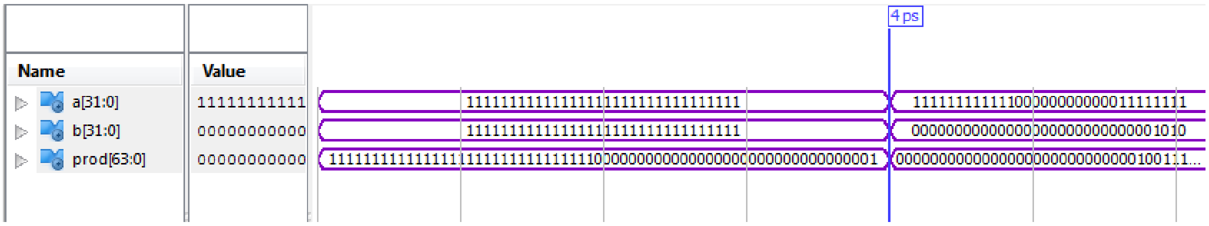

Figure 6: Waveform for 32-bit by 32-bit Multiplier

CONCLUSION

This paper proposes improvement in the design of Wallace multiplier when considered with respect to the processing delay. Using 4:2 compressors in the partial product reduction stage along with full-adders and half-adders has proved to be advantageous in reducing the number of stages when compared with the conventional Wallace tree multiplier. Also, the delay occurring at the final summation stage has been minimised by the use of Kogge-Stone adder (a fast parallel prefix adder).

Further improvements in this design can be achieved by using modified Booth algorithm in generation of partial product (first stage).

REFERENCES

[1] Rajaram, Srinath, and K. Vanithamani. "Improvement of Wallace multipliers using parallel prefix adders." In *Signal Processing, Communication, Computing and Networking Technologies (ICSCCN), 2011 International Conference on*, pp. 781-784. IEEE, 2011.

[2] Vinoth, C., VS Kanchana Bhaaskaran, B. Brindha, S. Sakthikumaran, V. Kavinilavu, B. Bhaskar, M. Kanagasabapathy, and B. Sharath. "A novel low power and high speed Wallace tree multiplier for RISC processor." In *Electronics Computer Technology (ICECT), 2011 3rd International Conference on*, vol. 1, pp. 330-334. IEEE, 2011.

[3] Srinitha, S., and B. Sargunam. "Area effective and speed optimized fused Add-Multiply unit." In *Innovations in Information, Embedded and Communication Systems (ICIIECS), 2015 International Conference on*, pp. 1-6. IEEE, 2015.

[4] Ramanthan, P., P. T. Vanathi, Amaresh Chaubey, and N. Senthil Raja. "Decomposition algorithm for power delay product optimization in Wallace multiplier." In *Control, Automation, Communication and Energy Conservation, 2009. INCACEC 2009. 2009 International Conference on*, pp. 1-6. IEEE, 2009.

[5] Kumar, G. Ganesh, and Subhendu K. Sahoo. "Implementation of a high speed multiplier for high-performance and low power applications." In *VLSI Design and Test (VDAT), 2015 19th International Symposium on*, pp. 1-4. IEEE, 2015.

[6] Veeramachaneni, Sreehari, M. Kirthi Krishna, Lingamneni Avinash, Sreekanth Reddy Puppala, and M. B. Srinivas. "Novel architectures for high-speed and low-power 3-2, 4-2 and 5-2 compressors." In *VLSI Design, 2007. Held jointly with 6th International Conference on Embedded Systems., 20th International Conference on*, pp. 324-329. IEEE, 2007.

[7] Asif, Shahzad, and Yinan Kong. "Design of an algorithmic Wallace multiplier using high speed counters." In *Computer Engineering & Systems (ICCES), 2015 Tenth International Conference on*, pp. 133-138. IEEE, 2015.

[8] Rao, M. Jagadeshwar, and Souvik Dubey. "A high speed and area efficient Booth recoded Wallace tree multiplier for fast arithmetic circuits." In *Microelectronics and Electronics (PrimeAsia), 2012 Asia Pacific Conference on Postgraduate Research in*, pp. 220-223. IEEE, 2012.

[9] Waters, Ron S., and Earl E. Swartzlander Jr. "A reduced complexity wallace multiplier reduction." *Computers, IEEE Transactions on* 59, no. 8 (2010): 1134-1137.

[10] Yezerla, Sudheer Kumar, and B. Rajendra Naik. "Design and Estimation of delay, power and area for Parallel prefix adders." In *Engineering and Computational Sciences (RAECS), 2014 Recent Advances in*, pp. 1-6. IEEE, 2014.

[11] Aparna, P. R., and Nisha Thomas. "Design and implementation of a high performance multiplier using HDL." In *Computing, Communication and Applications (ICCCA), 2012 International Conference on*, pp. 1-5. IEEE, 2012.

[12] Mhaidat, Khaldoon M., and Abdulmughni Y. Hamzah. "A new efficient reduction scheme to implement tree multipliers on FPGAs." In *Design & Test Symposium (IDT), 2014 9th International*, pp. 180-184. IEEE, 2014.

[13] Asif, Shahzad, and Yinan Kong. "Analysis of different architectures of counter based Wallace multipliers." In *Computer Engineering & Systems (ICCES), 2015 Tenth International Conference on*, pp. 139-144. IEEE, 2015.

[14] Wallace, Christopher S. "A suggestion for a fast multiplier." *Electronic Computers, IEEE Transactions on* 1 (1964): 14-17.